APPLICATION NOTE 32

1.0 INTRODUCTION

Pulse width modulation (PWM) amplifiers require low pass filtering of the output to demodulate the PWM carrier. Some applications also utilize the filter as a way to achieve an impedance transformation which draws less power supply current than is delivered to the load. These filters can be as simple as a single inductor, to multiple LC nodes depending on the application. In some applications the load will have enough inductance to act as its own filter. Deciding on the type and size of a filter can be time consuming since the calculations can be tedious and often give component values that are not easily obtainable. This application note is an effort to reduce filter calculation time. Using the Apex Power Design tool, available at www.apexmicrotech.com. will further reduce time. Power Design.exe is a self-extracting Excel97 spreadsheet and will be used extensively in this application note.

2.0 FILTER TYPES

PWM filters are normally a low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 Hertz to the frequency of cutoff (F_C). This low attenuation region is called the pass band. Beyond the F_C, attenuation increases at a rate determined by the filter type and the number of poles (order). Figure 1 indicates the general response of the low pass filter.

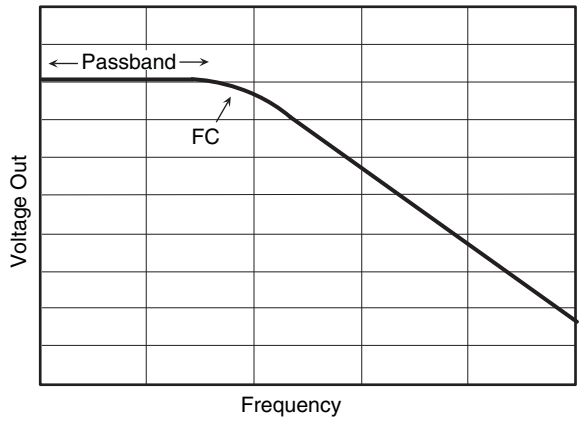

FIGURE 1. LOW PASS FILTER RESPONSE

Many different types of low pass filters exist. Each has favorable and unfavorable traits and the selection usually is a compromise of performance in one area to achieve desired performance in another area. Some characterizations are: pass band flatness, rate of attenuation, and phase shift versus frequency. Common filters include Butterworth, Chebyshev, and Bessel.

The Butterworth filter has a flat response in the pass band and good roll off beyond the cutoff frequency. Component variations do not greatly affect the performance. It is considered a good general filter that is often used and therefore will only be considered here.

3.0 INITIAL CONSIDERATIONS

If you are unfamiliar with Apex PWM amplifiers or with locked anti-phase modulation, please refer to Application Note 30. This should convince you that using unfiltered PWM outputs is useless for some loads (applies only full supply voltage) and can often be destructive to the load or the amplifier. Filter design requires trading off many variables. Here are some things to consider:

1. This filter design technique assumes amplifier output impedance is low compared to the load impedance and that the combined impedance of the load plus matching network is constant over frequency. The demand for circuit efficiency will insure the impedance relationship requirement is met. Beware that changing load element values, without corresponding matching network value changes, will alter the filter response curve. With some loads, such as solenoids or valves that tend to change inductance with position, the textbook response curve is nearly impossible to achieve. In these cases, try designing for the highest impedance, and then check performance driving the lower impedance.
2. As shown in Figure 2, a full bridge PWM amplifier driving a first order (single pole) filter with F_C set at 1/10, the switching frequency will be required to deliver approximately 15% of the peak output current as peak ripple current. The ripple is at the switching frequency; measured when the modulation level is 50%; and assumes peak output current equals Vs/R_L. Figure 2 also indicates that changing to a second or higher order filter will drop this to almost 10%. A second and even more effective way to reduce this ripple current is to widen the ratio between signal and switching frequencies. As switching frequencies of Apex PWM amplifiers range from 22.5KHz to 500KHz, this technique has obvious limits

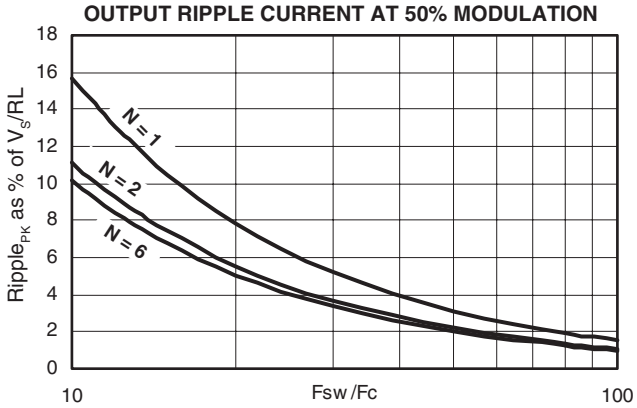

FIGURE 2. OUTPUT RIPPLE CURRENT VARIES WITH ORDER AND RATIO OF SWITCHING TO SIGNAL FREQUENCY

2.1 This ripple current flows through the first inductor of the filter, meaning high frequency core loss is of concern. With first order filters driving resistive loads, it also flows through the load. With higher order filters, most of the ripple current flows in the first filter capacitor, affecting the ripple capacity rating of these components.

2.2 In applications where full modulation is expected (output current is expected to approach V_S/R_L), the workload imposed on the amplifier by delivering the ripple current is of minor concern. While 15% (or less as shown in Figure 2) of maximum output may seem more than minor, Figure 3 shows this ripple current decreases as modulation percentage moves away from 50% (a graph of zero to 50% would

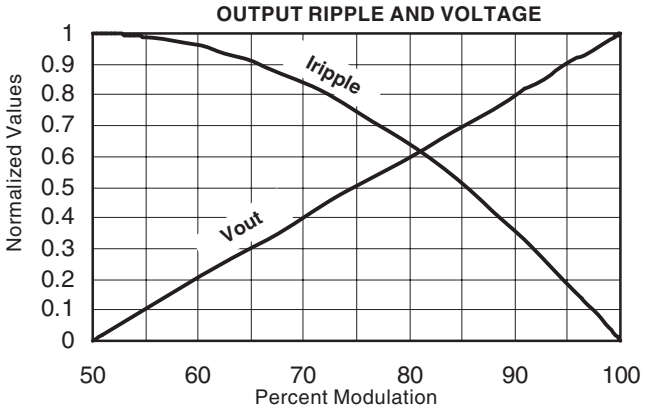

FIGURE 3. RIPPLE CURRENT AND OUTPUT VOLTAGE IN THE FULL BRIDGE

produce a mirror image curve) In other words, heatsink size is not increased 15% because maximum DC output and maximum ripple output never occur at the same time. The heatsink will be sized to handle the much larger output current. The ripple current curve of Figure 3 is also valid for half bridge circuits, but the Vout curve would need to be re-scaled from 0.5 at 50% modulation to 1 at 100%.

2.3 For applications spending a major portion of the time near the 50% modulation level, the ripple current will be quite noticeable in terms of lowered efficiency (power supply loading and heatsink temperature). These circuits include full bridges spending most of their time delivering small signals compared to peak output capability; full bridges whose peak output voltage is considerably less than supply voltage; and half bridges spending most of their time delivering half the supply voltage.

3. Filter attenuation at 100% of cutoff frequency is 3db, that is, a factor of 0.707 for voltage output (and consequentially, current) and 0.5 for power output. Refer to Figures 4 and 5 for more data on attenuation as signal frequency approaches cutoff frequency. Designing the cutoff frequency at least twice the actual maximum signal frequency is a very common technique to obtain a flatter response in the portion of the pass band actually used.

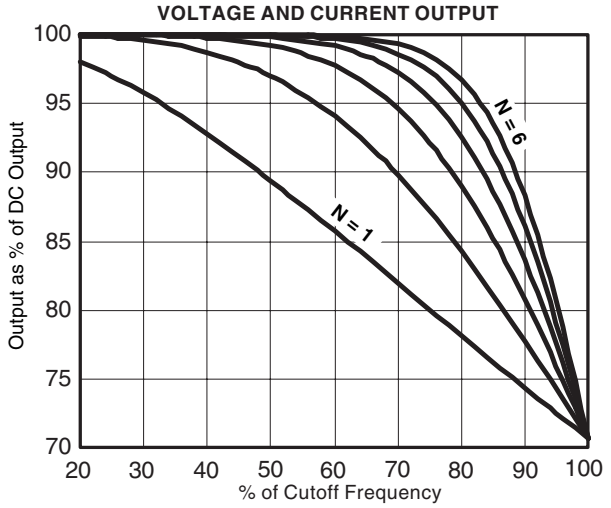

FIGURE 4. REDUCED V & I AS FSIGNAL APPROACHES Fc

4. With supply voltage and desired maximum ripple voltage at the load held constant, a larger ratio between signal frequency and switching frequency will lower the number of filter poles required. This will lower cost, weight and size.

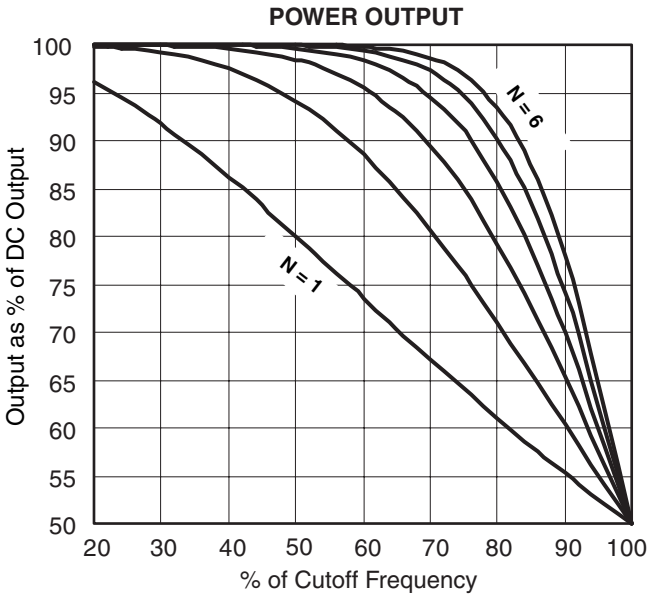

FIGURE 5. REDUCED POWER AS FSIGNAL APPROACHES FC

For example, starting with a 10:1 ratio requiring a 4 pole filter; changing to 21.4:1 brings N down to 3; and changing to 100:1 yields N=2.

5. In the design of servo loops or any other application where feedback is taken at the filter output or beyond, phase shift of the filter is critical to stability of the overall loop. With properly terminated filters, phase shift at the cutoff frequency will be 45° per pole and the shift will decrease in a linear fashion at lower frequencies. Power Design will calculate voltage and current phase shift at the load for all cases, but first and second order filters are likely to be the maximum acceptable. In fact, many designs use no dedicated filter components, but instead rely on load inductance and resistance to form a first order filter. The important point to check is how this inductance reacts to square waves of the switching frequency.

6. When using second and higher order filters, impedance presented to the PWM amplifier will dip below the load impedance as signal frequency approaches F_C. Figure 6 shows this in reciprocal form. Putting some numbers to go with the worst point: N=6, F_C=1KHz, F_{SIGNAL}=900Hz, I_{LOAD}=10A, amplifier output=12.3A. This "extra" current flows in the output devices of the PWM amplifier increasing

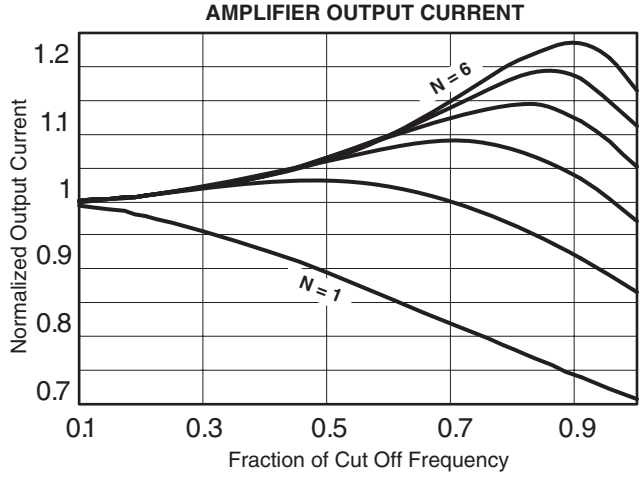

FIGURE 6. AMPLIFIER OUTPUT CURRENT CAN BE MORE THAN EXPECTED

internal power, increasing ON resistance, increasing junction temperatures and reducing efficiency. This effect should be considered also with regard to amplifier and power supply current ratings and design of current limit circuits. We will see what looks almost like a duplicate of this graph when discussing filter component stress levels.

Figure 7 shows efficiency data for a perfect component filter (no parasitics) designed for an SA03 running maximum output voltage into a 10Ω load while mounted on a 0.1°C/W heatsink. At 10% of F_C, about 3.3% is lost in the amplifier and the filter is having very little affect on efficiency. As signal frequency increases, three effects combine to bring high frequency efficiency down further. First, quiescent power remains constant even though the output signal is rolled off. Secondly, the peaking output current demanded by second and higher order filters increases internal PWM losses. The last item is the positive non-linear temperature coefficient of the ON resistance of the PWM, which increased about 1% in this example. The point here is that filter choices can double efficiency loss even before allowing for filter component loss. Importance of this data varies with the spectral content of the signal being amplified. Consider an audio application versus a fixed 400Hz inverter application.

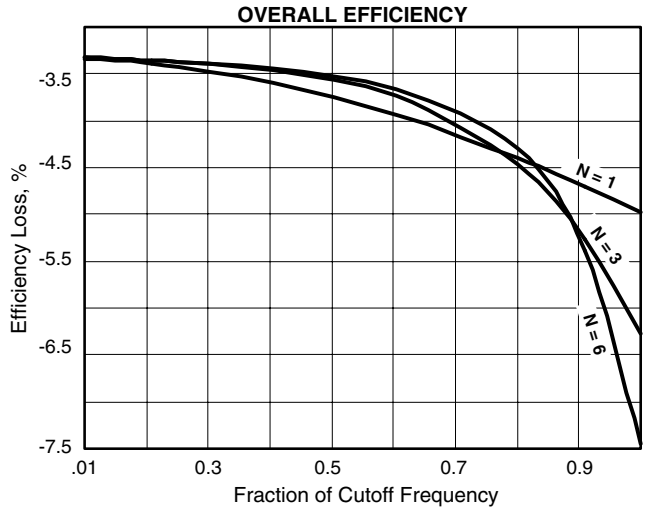

FIGURE 7. EVEN A THEORETICAL FILTER CAUSES REAL POWER LOSS

Desired attenuation of the PWM square wave output must be known to establish the order of the filter. While standard filter equations assume sine wave inputs, the PWM applies square waves at the switching frequency. Artificially increasing the bridge supply voltage by 25% approximates a correction factor for this. A non-integer value of this requirement is given in the following equation:

$$N \frac{\frac{A}{10}}{2 \bullet \text{LOG}\left[\frac{F_X}{F_C}\right]}$$

Where:

A (in db) = 20 log (bridge supply voltage * 1.25/load peak ripple voltage)

F_X = frequency of the desired attenuation (usually the switching frequency)

F_C = filter cutoff frequency

N is rounded up to the next integer

Note that ripple voltage on the load is a differential specification. With a full bridge circuit, it is not the voltage seen at either load terminal with respect to ground.

4.0 FILTER TABLES

Filter analysis begins by developing general mathematical equations to describe the filters. Each filter equation can be reduced to a set of coefficients.

Filter coefficient tables are usually in a normalized form. Normalized coefficients are calculated at a frequency of 1 radian per second and an impedance of 1 ohm. This is done for convenience so the designer does not have to calculate coefficients for every case. The normalized coefficients require the designer only to scale the frequencies and impedances to fit the particular requirement.

The filters most designers are familiar with are the symmetrical load type. These assume equal terminations on both ends of the filter. These configurations will generally not work here because the output impedance of the amplifier bridge is usually low and the actual load usually will be much higher. Apex PWM amplifiers have room temperature output impedances from less than 0.1 ohm to about 1 ohm and are mostly resistive. The filter tables here assume a very low source impedance and a higher impedance load.

The coefficient table also assumes zero loss components; therefore, real components will compromise results.

Filter orders up to 6 are given which is more than what is usually needed. Beyond order 5 or 6, the point of diminishing returns begins as losses in the filter components, parasitics of the physical layout, and undesired coupling eat up all the theoretical advantages of additional poles.

The single-ended filter configuration is shown in Figure 8. A first order filter would use only L1, a second order adds C1, a third order adds L2, and so on. The coefficients of Table 1 are used directly to find values for these filters. This configuration must be used with half bridge circuits and can be used with full bridge circuits by substituting the second PWM output for all the ground connections. This substitution is very rarely done because it places the high speed square waves of the PWM output on both load terminals and all the cabling between the amplifier and load. With rise and fall times usually in the tens of nanoseconds, and amplitude nearly equal to supply voltage, this is an extreme RFI problem

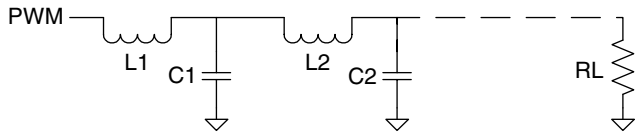

FIGURE 8. FOURTH ORDER, SINGLE-ENDED FILTER CONFIGURATION

ORDER	L1	C1	L2	C2	L3	C3
1	1					
2	1.4142	.7071				
3	1.5	1.3333	.5			
4	1.5307	1.5772	1.0824	.3827		
5	1.5451	1.6944	1.382	.8944	.309	
6	1.5529	1.7593	1.5529	1.2016	.7579	.2588

$$L = \frac{COEF * R_L}{2 * \pi * F} \qquad C = \frac{COEF}{2 * \pi * F * R_L}$$

L in Henries
C in Farads
R_L in Ohms

TABLE 1. FILTER COEFFICIENTS

5.0 FULL BRIDGE FILTER TOPOLOGIES

With full bridge circuits, an additional filter requirement is introduced in that common mode voltage applied to both load terminals usually needs to be minimized. The technique to achieve low common mode voltage is to simply split the inductor values in half, applying half to each PWM output as

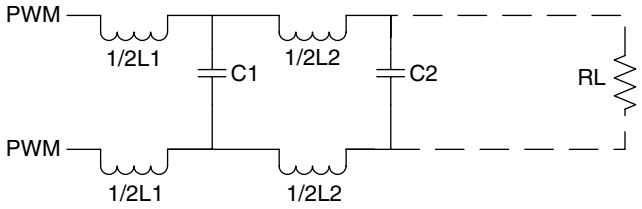

FIGURE 9. BASIC SPLIT INDUCTOR TOPOLOGY FOR THE FULL BRIDGE

shown in Figure 9.

If one could acquire a perfect PWM amplifier (equal rise and fall times, no dead time plus an exact out of phase condition), this filter would output common mode voltage proportional to inductor mismatch only. With real PWM amplifiers, the output will contain large amounts of high frequency harmonics. Each application is different, but peak-to-peak noise amplitude may approach the supply voltage. The spectral content of this noise extends well above the switching frequency. A pair of small capacitors added from the output side of each half of L1 to ground, as shown in Figure 10, will remedy this problem. It is not necessary (and sometimes it is counterproductive) to use more than this one pair of leg capacitors. Placing these small capacitors on the load side of L2 or L3 is not as effective as the placement shown.

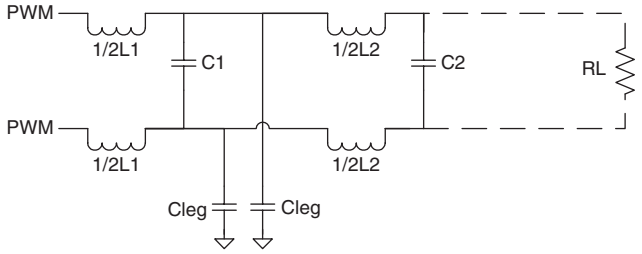

FIGURE 10. GROUND LEG CAPACITORS FILTER HIGH FREQUENCY COMMON MODE NOISE

Value selection for these ground leg capacitors is less critical than for the main filter capacitors. It has been determined empirically that setting the impedance value of these capacitors at the cutoff frequency, to between 10 to 30 times the value of the load resistance will provide reasonable common mode filtering. The addition of these capacitors will typically produce no more than 0.05db peaking, nor more than 0.2db change at the cutoff frequency in any order filter. From the technical point of view, the two Clegs are in series, and this is in parallel with C1. This means that on all but first order filters, C1 could be reduced by half the value of Cleg to eliminate even these small errors. Figure 11 shows the results of the following equation where the impedance ratio was set to 23:1:

$$C = \frac{1}{145 \bullet FC \bullet RL}$$

From a practical point of view, the lower left quadrant of this graph is textbook material only when using second and higher order filters. C1, C2, and C3 must be capable of bipolar operation and will be an order of magnitude or more larger than the leg capacitors. While the bipolar capacitors exhibit very low ESL and ESR to provide good roll off in the high frequency spectrum, this leads to very large and expensive banks of capacitors.

We previously noted that the two ground leg capacitors form an equivalent capacitor one half the value of the two individual devices. Carrying this thought a little further, we arrive at the common topology shown in Figure 12 where only unipolar capacitors are used, and where very good common mode

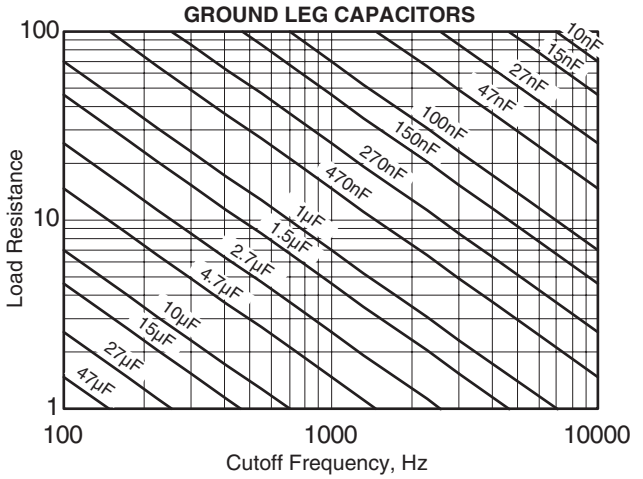

FIGURE 11. GROUND LEG CAPACITORS FOR COMMON MODE FILTERING

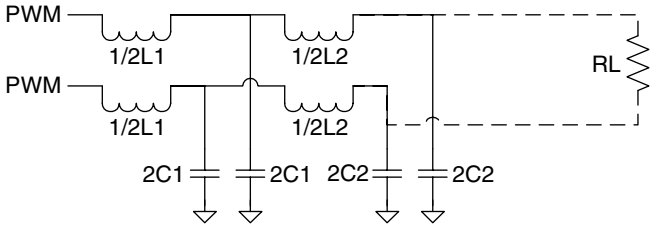

FIGURE 12. DUAL CAPACITOR TOPOLOGY MAY ALLOW UNIPOLAR CAPACITORS

filtering is inherent.

Do not assume this dual capacitor topology is a panacea for all high current, low frequency filters. The total amount of capacitance increases fourfold over the single capacitor topology. Additionally, the high frequency performance of these large unipolar capacitors tends to fall off more rapidly than bipolar varieties (ESL and ESR rise faster). As the two capacitors are in series, the equivalent ESL and ESR are TWICE the individual values rather than half. If maximum high frequency attenuation is required, large high quality bipolar capacitors are a must.

The dual capacitor topology using unipolar capacitors always works with second order filters and may work with higher order filters. Be sure to read section 6.0 FILTER COMPONENTS, where we will find it is very common for higher order filters to apply negative voltage to these capacitors.

6.0 REACTIVE LOADS

One more time: to achieve these filter responses a constant and purely resistive load termination is required. If a reactive load can be modeled as resistance in series with either capacitance or inductance, a simple conjugate match network can be used as shown in Figure 13. The resistor in the network will equal the resistor of the load model. As the network is in parallel with the load, all signals in the pass band will be applied to the network and power dissipation must be

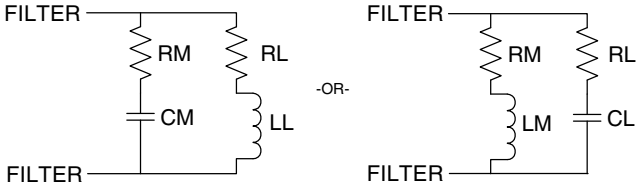

FIGURE 13. CONJUGATE MATCHING NETWORKS

checked. Realize that combined impedance of the network plus load is constant and that changing frequency shifts the power between the network and the load. This means a 100W capacitive load drive will require a 100W matching network if DC signals are allowed.

The Power Design frequency sweep capability will prove quite useful in determining power dissipation and in possibly choosing a non-perfect network trading off lower power dissipation for some distortion of the ideal filter response curve. Figure 14 illustrates one response example where the ideal match network resistor was doubled to reduce power dissipation. It is perfectly acceptable to omit the network as long as the resulting attenuation curve is also acceptable.

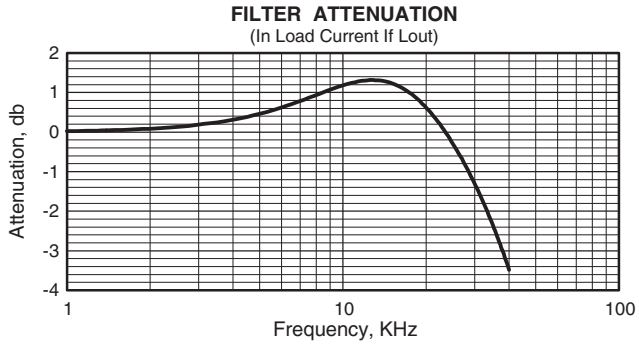

FIGURE 14. TRADING MATCH NETWORK POWER FOR SOME PEAKING OF THE FILTER

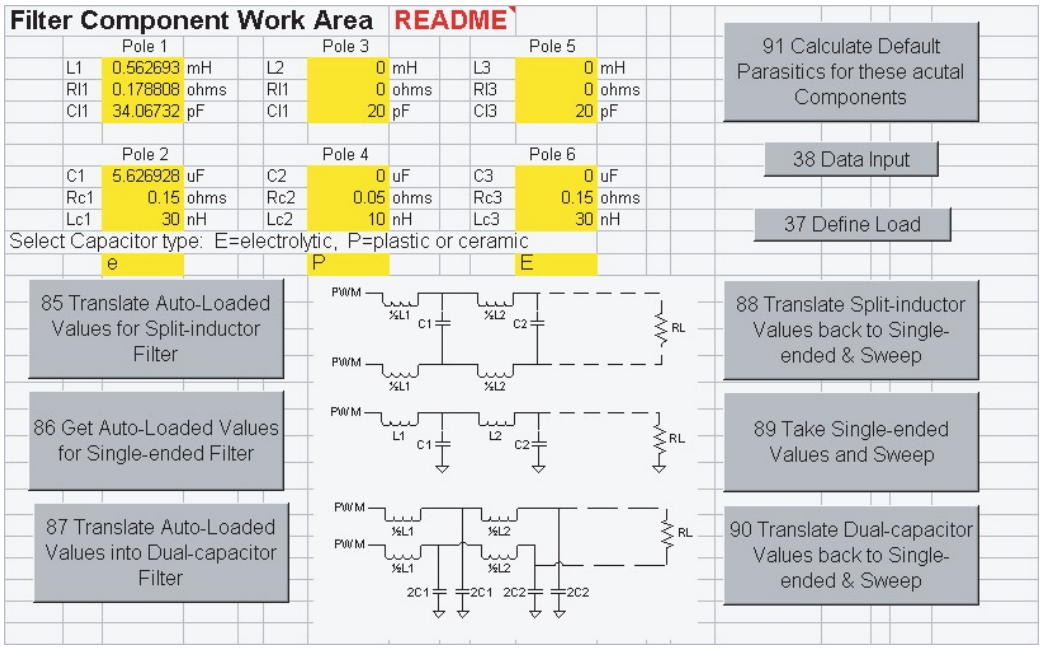

FIGURE 15. TRANSLATING VALUES FOR THE THREE TOPOLOGIES AND DEFAULT PARASITIC CALCULATION

7.0 FILTER COMPONENTS

Filters used in high power switching circuits often are the largest physical part of the circuit. Expect the filter to occupy more space than the rest of the circuitry. Expect currents and voltages to be greater than the output signal.

Filter components should be low loss, high current, high frequency devices. Check current ratings carefully as different manufacturers can use different rating methods. Make sure the inductors chosen have the required inductance at the maximum rated current and at the square wave switching frequency (many inductors are rated only with sine waves applied). We have seen laminated steel core inductors destroy circuits even when cutoff frequency was only 100 Hz! Successful applications usually implement powdered iron, ferrite, or air cores.

Polyester, polycarbonate, polypropylene, and chip ceramic capacitors are often used in the best PWM filters. Tantalum (preferred if voltages and temperatures allow) or electrolytic capacitors may be required in low frequency filters. The capacitors should have low loss at the switching frequency and well beyond (to at least the tenth harmonic).

While there is absolutely no substitute for finding real parasitic values for filter components, Power Design provides a default parasitic calculator for first pass design efforts, as shown in Figure 15. Parasitics vary WILDLY form part to part. The default calculator is ONLY intended to get somewhere in the pall park. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse.

Consult manufacture's data sheets or measure the parts to get accurate data.

Components loaded into this sheet by the PWM Filters sheet are for single-ended filters (to minimize spreadsheet size and sweep execution time). Use buttons 85-87 to put physical component values here for the type of filter you intend to build. Values to design single-ended filters will not be changed. For split-inductor designs, L will be divided by 2. For dual-capacitor designs, L will be divided by 2, plus C will be doubled.

Enter actual parasitics or calculate default values with button 91.

Use buttons 88-90 to re-load into the filter/load area and run the sweep. Values for Single-ended designs are not changed. For split-inductor designs, L and the parasitic R will be doubled plus parasitic C will be divided by 2. For dual-capacitor designs, inductors will be treated the same as for split-inductor designs and C will divided by 2, plus parasitic R & L will be doubled. Please note that even when using similar quality capacitors, the Q of a dual capacitor equivalent of a single capacitor is likely to be four times lower.

The folly of ignoring parasitics is illustrated by the data in Table 2. A second order filter was designed to provide 100.9db attenuation at the switching frequency. Using default parasitics, attenuation is listed for the three filter topologies using electrolytic and plastic capacitors.

TOPOLOGY	ELECTROLYTIC	PLASTIC
Split-inductor	68.1db	81.8db
Single-ended	68.6db	82.4db
Dual-capacitor	62.4db	75.3db

TABLE 2. COMPARING FILTER TOPOLOGY AND CAPACITOR TYPES

There are two conclusions to draw from this data: first, plastic capacitors have a definite advantage over electrolytic types. Secondly, the dual-capacitor topology is inferior to the other two. In a related issue, do not fall into the trap of thinking that adding a small high frequency capacitor in parallel with a much larger one having poor ESR and ESL will regain the ideal attenuation. Adding a plastic or ceramic capacitor equal to 1/10 the value of the large electrolytic brings attenuation up to only 81.1db for the split-inductor topology, still almost 20db short of ideal.

7.1 FILTER COMPONENT STRESS LEVELS

Multi-pole filters are a combination of one or more series resonant circuits and they do develop currents and voltages above the input and output levels as the signal frequency approaches the cutoff frequency. The highest stress levels will be born by L1 and C1. Higher order filters produce higher amplification levels. The last two components of the filter do not see stress levels above the signal level. Figure 16 illustrates these stress levels for L1, L2, C1, and C2 for all filter orders up to 6. Voltages and currents are normalized to the DC or very low frequency output signal amplitude and are based on ideal components.

Data on current can be used directly for any filter topology for both inductors and capacitors. If a split inductor topology is used, the inductor voltage data must be divided by two. Voltage data can be used directly for capacitors not connected to ground. Ground terminated capacitors have a DC bias equal to 1/2 the supply voltage which must be added to half the peak voltage calculated from the graphs. To find peak capacitor voltages the equation is:

$V_{PEAK} = Vs/2 + Vout_{PEAK}/2$ * graph reading

Do this calculation for BOTH the positive and negative peak output voltages. Note that if output voltage is nearly equal to supply voltage, and the filter order is three or more, the most negative going peak for C1 will be negative with respect to ground. The same is true for C2 with fifth and sixth order filters. This means even a ground-terminated capacitor can have BIPOLAR voltages applied. From a practical point of view, this situation implies the use of unipolar capacitors limits filter order to two.

As an example, consider filter options for an SA06, which is to deliver ±470V to a 332Ω resistive load at 1KHz. Current will be 1.414A peak or 1A RMS. Power will be 665W peak or 332Wrms. A supply of 480V will provide plenty of headroom for internal losses and maximum linear duty cycle limitations. The worst case for voltage and current extremes will be a sixth order filter.

L1 peak current = 1.414A * ~1.23 = 1.75A
L1 peak voltage = 470V * ~1.82 = 850V
C1 RMS ripple current = 1A * ~1.82 = 1.82A
C1 peak voltage (differential) = 470V * ~1.17 = 548V
C1 + peak voltage (grounded) = 240V + 274V = 514V
C1- peak voltage (grounded) = 240V - 274V = -34V Must be bipolar

The same math with graph values from the other four graphs will yield stress levels for L2 and C2.

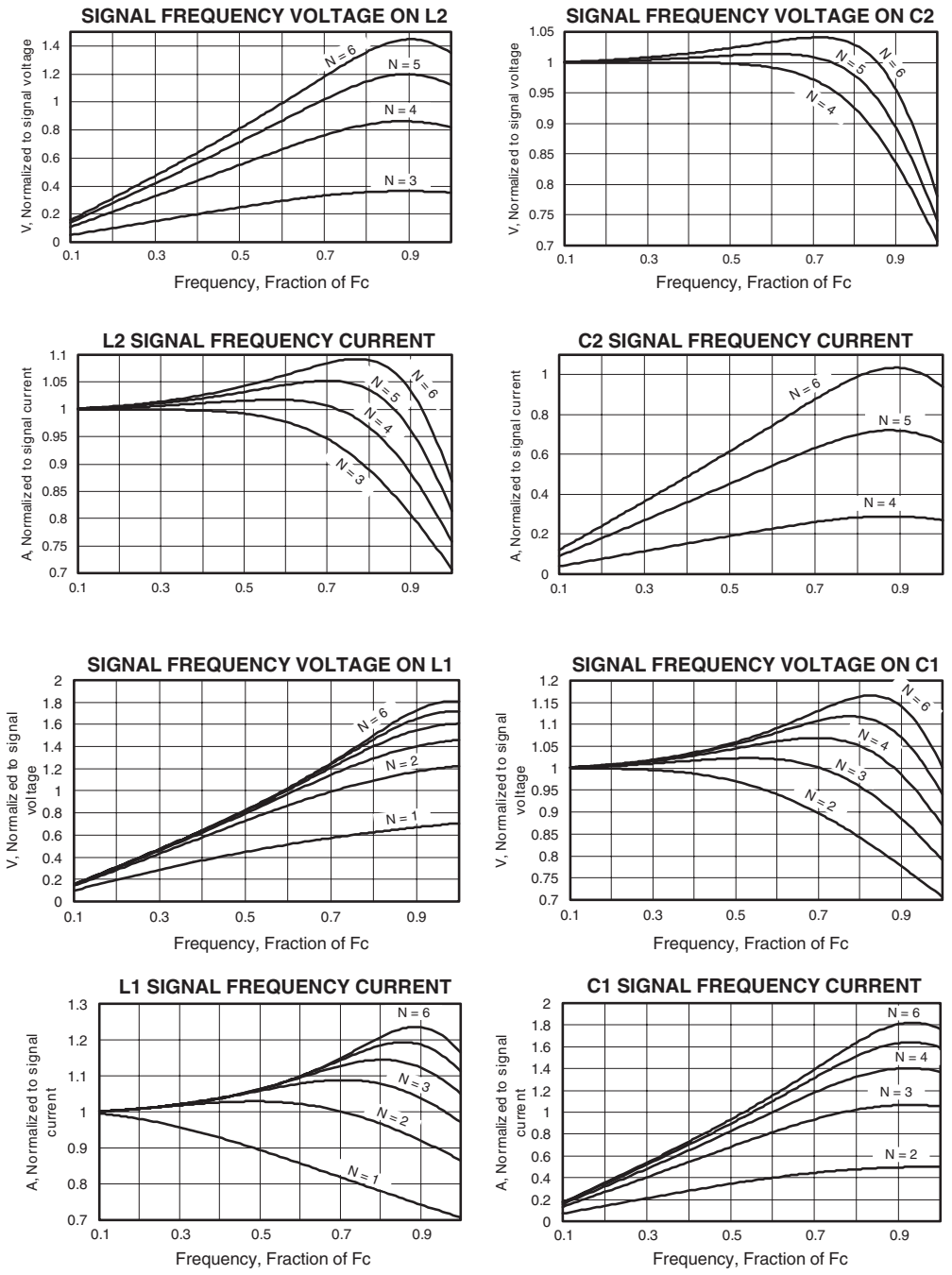

FIGURE 16. FILTER COMPONENT STRESS LEVELS

We can now make some general statements about filter design. Higher order filters can increase component ratings by as much as 82%. The two most costly increases are first, the ripple current on C1 and then the voltage rating of L1. While lowering filter order helps this situation, an even better way to minimize component requirements is to design the cutoff frequency as a multiple of the maximum input signal frequency. Turning this around, limiting input signal to one half or less of the cutoff frequency, limits these stress level increases to about 6% for sixth order filters and even less for more moderate (and practical) orders. Figures 17 and 18 show the Power Design answers for L1 and C1 stress levels of this example modified for a cutoff frequency of 2KHz rather than 1KHz. An additional benefit of this change is a 2:1 reduction in the values of filter components. The performance cost of this change at the switching frequency is a reduction of attenuation equal to 6db for each order (@ N=4, -108db drops to -84db).

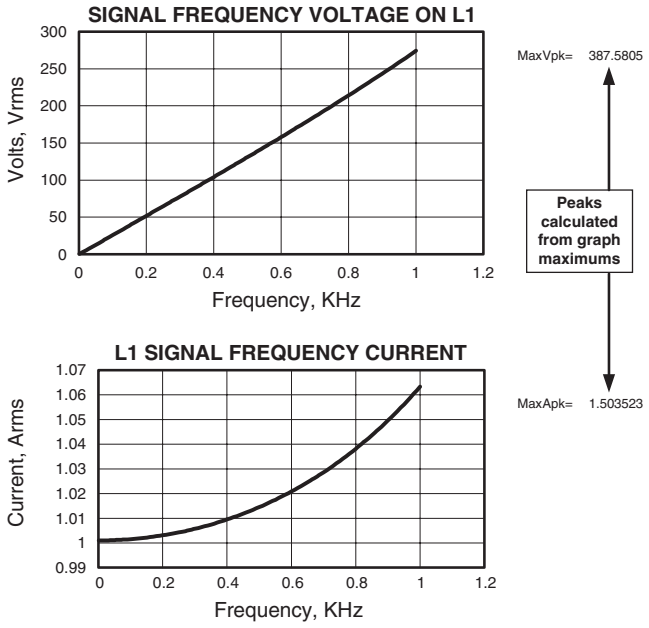

FIGURE 17. DOUBLING Fc LOWERS L1 STRESS LEVELS

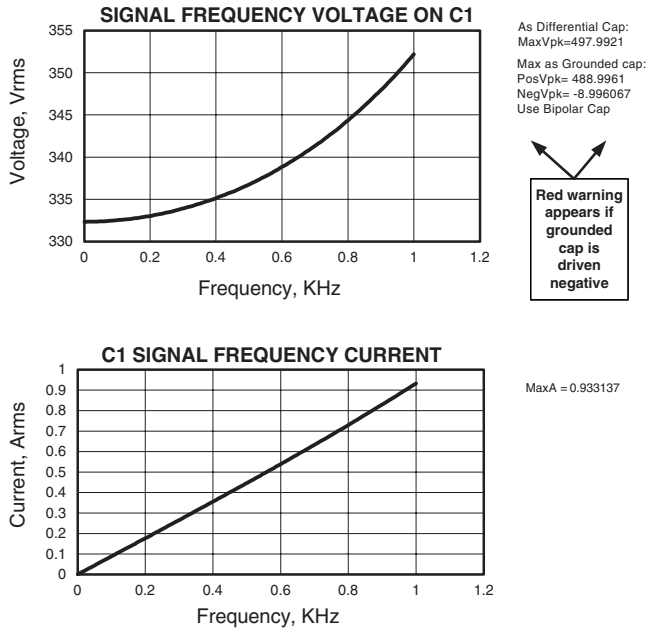

FIGURE 18. DOUBLING Fc LOWERS C1 STRESS LEVELS

8.0 SAFETY CONCERNS

A word of CAUTION. These graphs were generated with perfect components giving the best possible circuit Q, compared to real components having losses and therefore generating lower peaks. On the opposite side, these graphs reflect perfectly terminated filters; and normal component tolerances destroy this perfection. Do NOT power up filters unless your are sure they are properly terminated. Use Power Design to **CHECK COMPONENT TOLERANCES.**

These graphs also assume sine wave inputs (the only waveform Power Design deals with). Figure 19 is a Spice simulation of this original example showing L1 and C1 stresses when the input signal is a 900Hz, 470V square wave. L1 voltage = ±582V and is for 1/2 the total inductance. L1 current peaks at ±2.14A. C1 current peaks at ±3.18A. C1 is grounded and has voltage peaks of 587V and -107V. The output is a very good looking sine wave instead of a square, and peak amplitudes have risen from 470V to 527V, from 1.414A to 1.59A and from 665W to 838W.

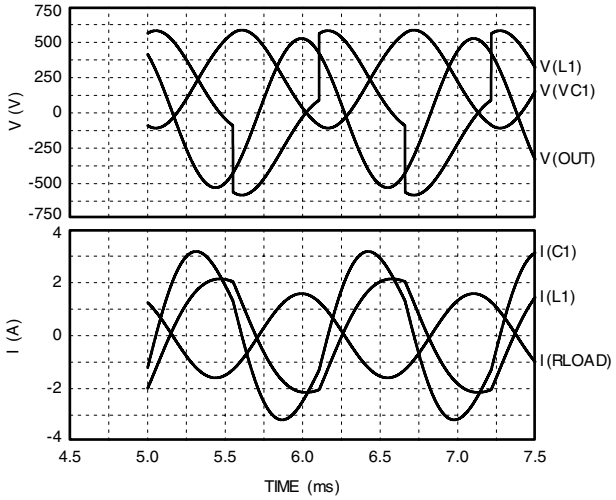

FIGURE 19. SQUARE WAVES THROUGH A 6 POLE FILTER COME OUT AS LARGER SINE WAVES

9.0 EXAMPLES

Example 1. The voice coil of a shaker table has 7Ω resistance and 100uH inductance. The desired drive level is 50V peak from 10Hz to 2KHz. Starting with the Power Design, Part Selection sheet, SA60, PA93, PA04, and SA01 are the first choices in order of cost. SA60 was rejected because it has no current limit. In the Power sheet, it takes only about a minute to find that the PA93 cannot handle the internal power dissipation (about 140W). Switching to PA04 reveals the circuit is possible, but would require a 0.2°C/W heatsink to keep junction temperatures to 150°C and has efficiency in the 50% area. This temperature may not be acceptable from a reliability point of view and leaves poor choices for the heatsink. Choice one is the Apex HS11 with liquid cooling; read this as costing nearly as much as the amplifier before calling a plumber. Choice two involves a custom heatsink.

The SA01 PWM amplifier is the most cost effective choice and will run much cooler. With PWM amplifiers, a power supply voltage substantially higher than peak output voltage is not a killer in terms of internal power dissipation. This allows an 80V unregulated supply, saving a lot in terms of efficiency, cost and design time over a regulated supply required by a linear solution. The SA01 circuit will follow the voltage control example given in Application Note 30 PWM BASICS. It was determined that 150mV peak ripple at the 42KHz switching

frequency would be acceptable. In order to maximize pass band flatness and avoid the numerous pitfalls of driving signals right up to the cutoff frequency, Fc will be designed for 4KHz. Figure 20 shows this data loaded into the PWM Filters sheet of Power Design.

Filter Design for PWM Amplifiers READ ME

CAUTION! Refer to Applications Note 32

Input Data

Model	SA01				
Vs	80	Volts			
Fsw	42	KHz	42	N(exact)	2.7653
Fmin	0.01	KHz			
Fmax	2	KHz		N(recommended)	3
Fcutoff	4	KHz			
Rload	7	Ohms			
Cload	0	uF			
Lload	0.1	mH			
Vripple	0.15	Vpk			
Signal	50	Units			
Sig as ?	V peak	Note/W			

Order Calculation

Atten. @ Fsw 56.478 db

Matching network

Cm = 2.0408 uF

Lm = 0 mH

Rm = 7 Ohms

Read Me

Notes: SA01 Shaker Table Example

46 Print Filter | 55 Show Attenuation in db & % | 56 Show Attenuation Graph | 66 Show Filter Components

Using the Complex Load:

60 Load All Data For N=1 | 61 Load All Data For N=2 | 62 Load All Data For N=3 | 63 Load All Data For N=4 | 64 Load All Data For N=5 | 83 Load All Data For N=6

No Auto Sweep on Load?

FIGURE 20. SETTING UP THE PWM DESIGN FOR ANALYSIS

Figure 21 gives all the component choices for the third order filter. If a single ended filter was desired, components under that heading would be used. If a dual capacitor topology is desired, use components from the dual cap column. To form the most common topology, the split inductor, this example will use inductors from the differential column and capacitors from the single-ended column. Leg capacitors will be 0.27uF per Figure 11. The 2.28Ap-p ripple will be the maximum ripple in L1 at the switching frequency. The 0.57A is used to calculate power loss in the amplifier.

Shading indicates values for Split Inductor topology

		Dual Cap Filter		Single-ended Filter	
N = 3	L1 =	0.2089	mH	0.4178	mH
	C =	15.157	uF	7.5786	uF
	L2 =	0.0696	mH	0.1393	mH

P-P Iripple = 2.2796 Amps out of the amplifier

Avg. Iout for thermal calculations = 0.5699

FIGURE 21. THIRD ORDER DATA ONLY FROM THE COMPONENTS SCREEN

The inductors will be custom wound. L1s are 47 turns of #12 on a Micrometals T184-18 torriodal core. L2s are 39 turns of #12 on a T130-18 core. The single ended capacitor is metal-

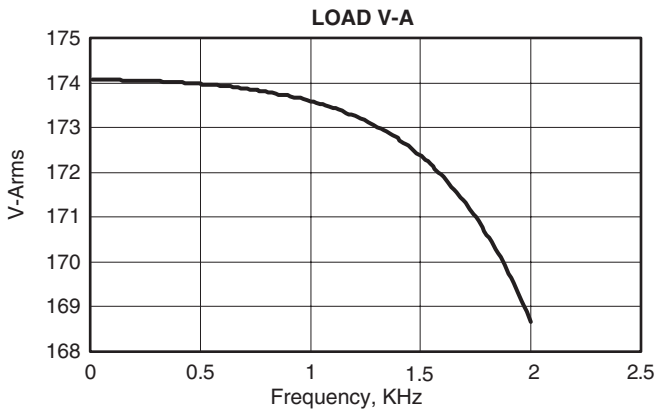

FIGURE 22. POWER DELIVERY TO THE SHAKER TABLE

lized polypropylene and the leg capacitors are X7R ceramic. The matching network capacitor is a pair of 1uF, X7R ceramics in parallel. Figure 22 shows the delivered power to be about 2% low at the lowest frequencies. This is primarily from copper loss in the inductors and suggests a simple gain adjustment be included in the circuit. At first glance the power roll-off at 2KHz looks a bit large. However a linear sweep analysis of a perfect drive to the voice coil reveals the coil inductance itself is responsible for over half this droop.

With your own copy of Power Design, you will use the PWM Power sheet to find the SA01 delivers full power while averaging an internal loss of under 15W. When mounted on the Apex HS16 without a fan, the SA01 will have a case temperature rise of only 19°C and junctions only 3°warmer. Adding in filter loss (including the matching network) as shown in Figure 23, still yields efficiency better than 92% over most of the frequency band.

Example 2. This example illustrates the transformer-like action of a PWM system. The requirement is to drive a 2Ω thermo-electric cooler at ±10V, using an existing single 48V supply. Any linear solution will draw 5A or 240W from the

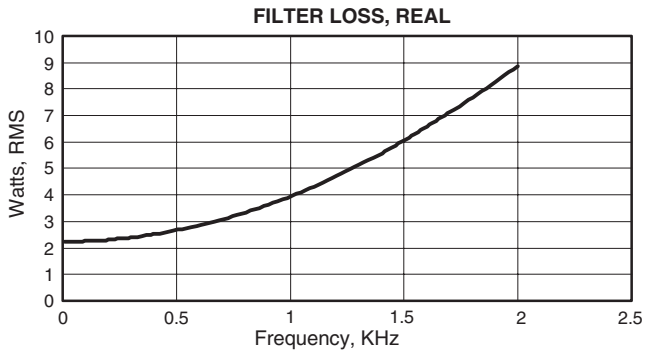

FIGURE 23. POWER LOSS IN THE FILTER AND MATCHING NETWORK

supply and will need to dissipate 190W. SA60 is the least expensive PWM amplifier having analog input capability. A 10Hz bandwidth will be plenty and ripple voltage should be kept below 100mV across the cooler. It is also desirable to keep the common mode ripple as low as possible, so a dual capacitor filter will be considered. A first pass with the PWM Filter sheet loaded with switching frequency=45KHz and cutoff frequency=100Hz, called for inductors of 2.25mH and capacitors of 1125uF. The large capacitance values suggest electrolytic types which generally offer lower performance in the high frequency spectrum. A second pass at the design set cutoff frequency at 1KHz, yielding the data in Figure 24.

Shading indicates values for Split Inductor topology

		Dual Cap Filter		Single-ended Filter	
N = 2	L =	0.2251	mH	0.4502	mH
	C =	112.54	uF	56.269	uF

P-P Iripple = 1.1848 Amps out of the amplifier

Avg. Iout for thermal calculations = 0.2962

FIGURE 24. CHANGING Fc TO 1KHz YIELDS MORE REASONABLE COMPONENT VALUES

In checking available metallized polypropylene capacitors, it was discovered that a single-ended capacitor would cost less than a third that of the pair of dual value capacitors. The final filter shown in Figure 25 is a hybrid where the table for

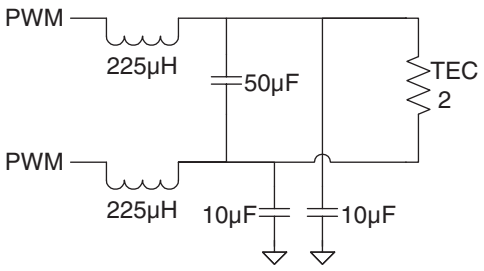

FIGURE 25. A CROSS BETWEEN SPLIT INDUCTOR AND DUAL CAPACITOR TOPOLOGIES

leg capacitors is ignored and the three capacitors form the equivalent of a 55uF single capacitor and provide excellent common mode attenuation.

Figure 26 illustrates finding default parasitics and loading equivalent components to run the frequency sweep on. In the Filter Component Work Area, enter values by hand and then use button 91 to calculate the parasitics. Note the 0.1Ω and 23nH values calculated for the 10µF capacitors. The equivalent single-ended capacitor has half the capacitance and twice the resistance and twice the inductance. Translate back to single-ended with button 88 and return to the Define Load area when the sweep is complete. Now enter the equivalent values for the pair of 10µF capacitors as shown in Figure 27, and run the sweep.

Filter Component Work Area		README					
	Pole 1		Pole 3			Pole 5	
	L1	0.225 mH	L2	0 mH		L3	0 mH
	Rl1	0.0775 ohms	Rl1	0 ohms		Rl3	0 ohms
	Cl1	25.625 pF	Cl1	20 pF		Cl3	20 pF
	Pole 2		Pole 4			Pole 6	
	C1	50 uF	C2	10 uF		C3	0 uF
	Rc1	0.134949 ohms	Rc2	0.1 ohms		Rc3	0.15 ohms
	Lc1	32.08661 nH	Lc2	23 nH		Lc3	30 nH
Select Capacitor type: E=electrolytic, P=plastic or ceramic							
	p		P			E	

FIGURE 26. FINDING DEFAULT PARASITICS FOR A HYBRID FILTER TOPOLOGY

Pole 1		Pole 3	
L1	0.45 mH	L2	0 mH
Rl1	0.155 ohms	Rl1	0 ohms
Cl1	12.8125 pF	Cl1	5 pF
Pole 2		Pole 4	
C1	50 uF	C2	5 uF
Rc1	0.134949 ohms	Rc2	0.1 ohms
Lc1	32.08661 nH	Lc2	23 nH

FIGURE 27. MANUAL ENTRY OF COMPONENT EQUIVALENTS FOR A HYBRID FILTER TOPOLOGY

Now for the real beauty of this circuit: when delivering the full 5A (50W), the SA60 mounted on an Apex HS03 1.7°C/W heatsink (needs a mounting hole drilled), has an internal dissipation of only about 15W! Throwing in filter loss also, the supply is working to the tune of only about 70W, or about 1.5A.

Example 3. This circuit drives a magnetic bearing requiring up to 12A DC plus up to 3A peak AC up to 300Hz. Bearing coil inductance is 5mH and resistance is 2Ω. Using the Power sheet reveals the AC drive will require 29Vpk, which brings total peak voltage up to 54V. As the PWM circuit will be inside a larger loop based on a position sensor, low phase shift is much more important than amplitude accuracy. The SA03 will handle this job using a current output circuit based on its data sheet typical application. Maximum 22.5KHz ripple voltage at the bearing is 1V peak. Knowing that filters shift phase the least amount in the lowest portion of the bandpass, it was decided to set the cutoff frequency to 3KHz. A split inductor topology will be used with N=3. This data was loaded into Power Design yielding 80uH for the L1s, 35uF for the capacitor, 27uH for the L2s, and 1250uF for the capacitor in the matching network. Leg capacitors will be 1uF. Figure 28 shows the initial current control results.

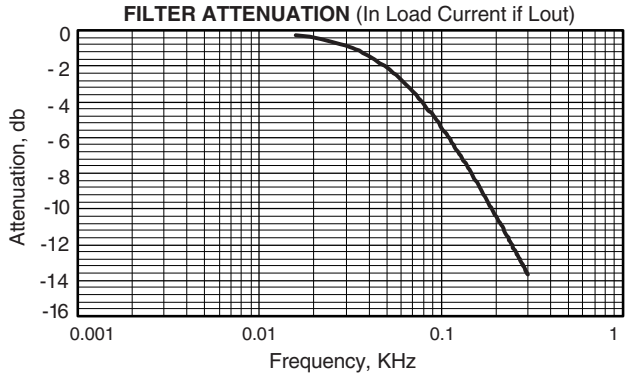

FIGURE 28. THIS IS IDEAL RESPONSE?

In checking the graph on load current, it agrees by saying current at 300Hz is down to about 20% of DC levels. The ideal filter keeps output voltage constant in the pass band. In this case the large inductance of the load called for an R-C matching network, which draws most of the current at 300Hz.

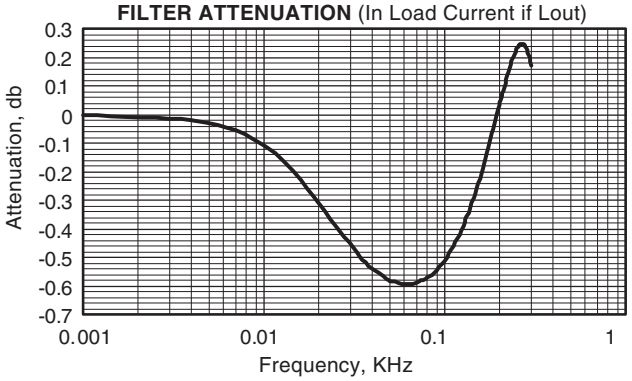

FIGURE 29. DB RESPONSE OF THE MODIFIED MATCHING NETWORK

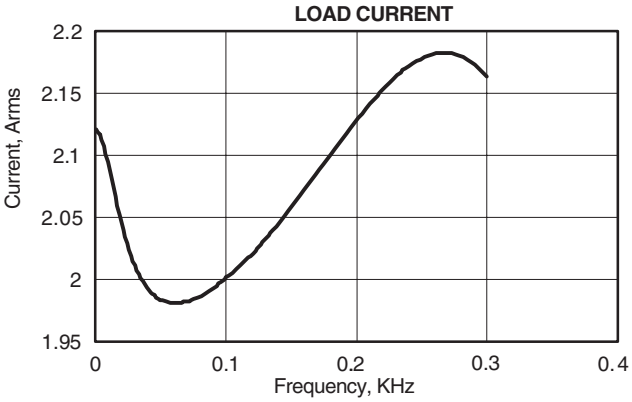

FIGURE 30. CURRENT OUTPUT WITH THE MODIFIED MATCHING NETWORK

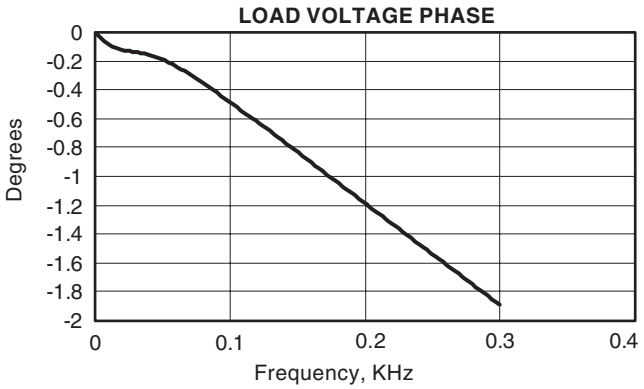

FIGURE 31. OUTPUT VOLTAGE PHASE WITH THE MODIFIED MATCHING NETWORK

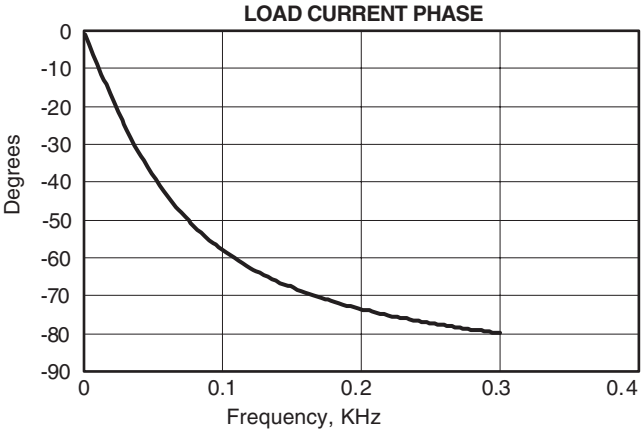

FIGURE 32. CURRENT OUTPUT PHASE WITH THE MODIFIED MATCHING NETWORK

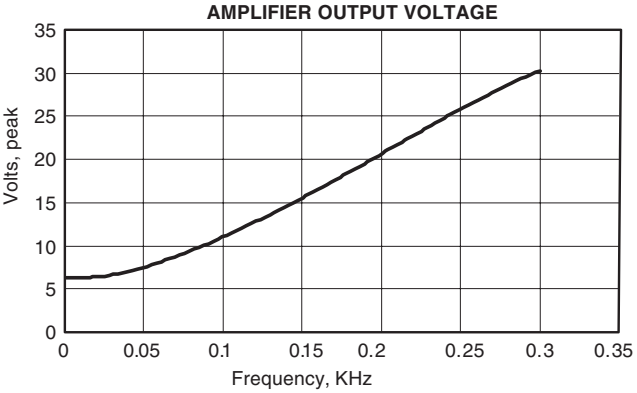

FIGURE 33. AMPLIFIER OUTPUT VOLTAGE WITH THE MODIFIED MATCHING NETWORK

We found earlier that removing a matching network causes voltage peaking at the filter output; this is exactly what we need to keep current constant due to the bearing inductance. Total removal causes about an 8db peaking (a gain of about 2.5), but a few iterations later, 470uF and 13Ω was found to produce the results shown in Figures 29-34.

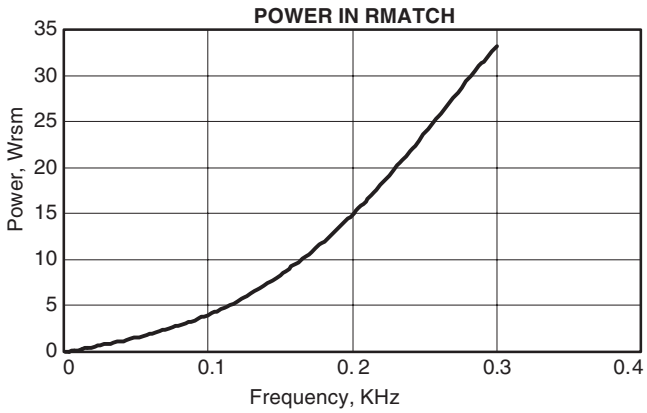

FIGURE 34. POWER DISSIPATION IN THE MODIFIED MATCHING NETWORK

To estimate internal power dissipation for the SA03, a new sweep was run with amplitude set to the RMS sum of 12A DC and 3Apk AC (~12.2Apk). Putting the 1.48°C/W minimum rating from this sweep into the Heatsinks sheet brings up the HS06 rated at .96°C/W. This will result in a case temperature a little over 60° and junctions a little over 70° at maximum drive.

10.0 FINAL CONSIDERATIONS

DO NOT DRIVE THESE FILTERS WITHOUT PROPER LOADING.

If you were taught to never have a load on a power circuit the first time you turn it on, be aware that the resonant circuits of these filters can generate voltages many times larger than the input voltage.

Poor circuit layout cannot be remedied by good filtering. PWM circuits, by their nature, have high frequency, and high power transients, that are difficult to eliminate from the desired output signal. Use ground planes and shielding as much as possible, but do not use these as a high current path. Use wide traces on circuit boards for power supply and output signals and heavy gauge wire for interconnects. Use star grounding techniques with the PWM amplifier ground pin as the center. A very small amount of inductance can cause large transients where high currents switch quickly. A rule of thumb is to expect 20nH per inch of conductor. Assume all output current changes its path through the PWM output switches each cycle of the switching frequency in 20 to 50ns. Space circuit board traces and wiring away from sensitive circuits to avoid extraneous noise pickup. Use bypass capacitors liberally.

The response curves for prefect components imply that the attenuation increases continuously with increasing frequency. With real components and real interconnects this is simply not the case. If you have a design claiming 150db attenuation, check it again.